

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Terrence C. Leslie	Examiner:	Matthew C. Landau
Serial No.:	10/765,301	Group Art Unit:	2815
Filed:	January 27, 2004	Docket:	303.860US1
Title:	SELECTIVE EPITAXY VERTICAL INTEGRATED CIRCUIT COMPONENTS AND METHODS		

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants hereby authorize the Commissioner to charge the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p), to Deposit Account No. 19-0743. Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

TERRENCE C. LESLIE

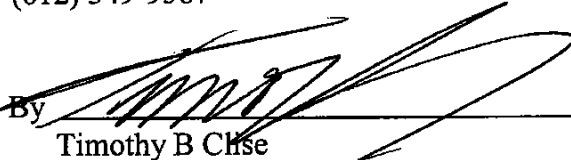
By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 349-9587

Date

4 May '06

By

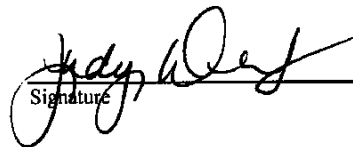


Timothy B Chase  
Reg. No. 40,957

**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31<sup>st</sup> day of May, 2006.

JUDY DETN  
Name

Signature



31<sup>st</sup> May 2006

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

<b>Application Number</b>	10/765,301
<b>Filing Date</b>	January 27, 2004
<b>First Named Inventor</b>	Leslie, Terrence
<b>Group Art Unit</b>	2815
<b>Examiner Name</b>	Landau, Matthew

Sheet 1 of 1

Attorney Docket No: 303.860US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date if Appropriate
	US-6,687,146	02/03/2004	Kurjanowicz, Wlodek , et al.	01/31/2002

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		DEFFREE, SUSAN , "IBM proves vertical transistor DRAM at 70nm", <u>Electronic News</u> , (June 10, 2003),2 pgs	
		HERGENROTHER, J M., et al., "The vertical replacement-gate (VRG) MOSFET: a 50-nm vertical MOSFET with lithography-independent gate length", <u>Bell Laboratories, Lucent Technologies, Murray Hill</u> , 4pgs	
		ISA, "IBM claims speediest silicon transistor", <a href="http://www.isa.org/Template.cfm?Section=Communities&amp;template=/TaggedPage/DetailDisplay.cfm&amp;ContentID=20445">http://www.isa.org/Template.cfm?Section=Communities&amp;template=/TaggedPage/DetailDisplay.cfm&amp;ContentID=20445</a> , ISA - The Instrumentation, Systems and Automation Society,(November 4, 2002),2 pgs	
		LUCENT TECHNOLOGIES, "Revolutionary transistor design turns the silicon world on end", <a href="http://www.bell-labs.com/news/1999/november/15/1.html">http://www.bell-labs.com/news/1999/november/15/1.html</a> , Lucent Technologies, Bell Labs Innovations,(1999),3 pgs	
		LUCENT TECHNOLOGIES, "Revolutionary transistor turns silicon world on end", (2000),2 pgs	
		NING, T H., "Why BiCMOS and SOI BiCMoS?", <u>IBM</u> , 0018-8646,(11.29.01),7 pgs	

**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.  
<sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached